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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,881	WILKERSON, CHRISTOPHER B.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *31-34* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *5,16,23 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-11, 19-22, 24-29 are rejected under 35 U.S.C. 102 (b) as being clearly anticipated by Ebcioglu et al., US Patent 5,799.179.

3. Referring to claim 1, Ebcioglu et al. have taught a method comprising:

a. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16); and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16);

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (column 4, lines 22-26, column 7, lines 13-16, column 9, lines 51-63, Speculative instructions that are outside of the taken path are discarded, or bypassed, because they are no longer needed.).

4. Referring to claim 2, Ebcioglu et al. have taught the method of claim 1, as described above, and wherein setting comprises setting the tag of a register when an instruction having the register as a destination results in a cache miss (abstract, column 3, lines 31-631-61, column 4,

lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16, column 7, lines 25-34, The tag registers are set in response to an exception. A cache miss is an exception.).

5. Referring to claim 3, Ebcioglu et al. have taught the method of claim 1, as described above, and further comprising: propagating the tag to destination registers of the instructions to indicate that an operand within the destination registers is a scratch value (column 3, line 30-column 4, line 40, The speculative bit for each instruction is propagated to all of the operand registers during the entire time the instruction is executed.).

6. Referring to claim 4, Ebcioglu et al. have taught the method of claim 1, as described above, and further comprising: bypassing execution of an arithmetic instruction having at least one register as an operand with an associated tag indicating that the register contains data that is a scratch value (column 9, lines 51-column 10, line 60); and bypassing execution of a store instruction involving a value derived from the register having an associated tag indicating that the register contains data that is a scratch value (column 9, lines 51-column 10, line 60).

7. Referring to claim 6, Ebcioglu et al. have taught the method of claim 1 as described above, and further comprising: marking each instruction in a pipeline with a tag to indicate if the instruction involves a scratch value (column 3, lines 30-45, Figure 1b).

8. Referring to claim 7, Ebcioglu et al. have taught the method of claim 1 as described above, and further comprising: propagating the tag through a store buffer if an address generation register does not indicate that the address generation register holds a scratch value (Column 5 lines 30-44, The 33rd bit.).

9. Referring to claim 8, Ebcioglu et al. have taught a processor comprising: a plurality of registers having a corresponding plurality of register tags to indicate whether the data stored in

the register holds a scratch value (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16, speculative register bits); a plurality of flags having a corresponding plurality of flag tags to indicate whether the data reflected by the flag is based on a scratch value (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16, speculative instruction bits, Figures 1a and 1b), and a plurality of predicates having a corresponding plurality of predicate tags to indicate whether the data reflected by the predicate is based on a scratch value (column 9, lines 5-7, column 7, lines 5-16, special purpose register speculative bits); and an execution engine to bypass execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (column 4, lines 22-26, column 7, lines 13-16, column 9, lines 51-63, Speculative instructions that are outside of the taken path are discarded, or bypassed, because they are no longer needed.).

10. Referring to claim 9, Ebcioglu et al. have taught the processor of claim 8, as described above, and having an instruction set including a plurality of instructions, each instruction augmented by an instruction tag to indicate whether the instruction involves a scratch value (Figures 1a and 1b, speculative bit).

11. Referring to claim 10, Ebcioglu et al. have taught the processor of claim 9, as described above, and wherein the register tags, flag tags, predicate tags, and instruction tags have a size of one bit (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16).

12. Referring to claim 11, Ebcioglu et al. have taught the processor of claim 9, as described above. Ebcioglu et al. have not specifically taught wherein the register tags, flag tags, predicate

tags and instruction tags have a size of at least two bits. However, having the tags be any size, including two or more bits, would have been obvious to one of ordinary skill in the art at the time the invention was made as it has been held that changes in size is not a patentable difference, see *In re Rose*, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).

13. Referring to claim 19, Ebcioglu et al. have taught a system comprising:

a. a memory, a storage device, and a processor each coupled to a bus (column 1, lines 40-59, Figure 2);

b. the processor including an execution engine having instructions which when executed by the processor cause the processor to perform actions including:

i. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16);

ii. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16); and

iii. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (column 4, lines 22-26, column 7, lines 13-16, column 9, lines 51-63, Tagged speculative instructions that are outside of the taken path are discarded, or bypassed, because they are no longer needed.).

14. Claims 20-22, 24 and 25 do not recite limitations above the claimed invention set forth in claims 2-4, 6, and 7, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 2-4, 6, and 7 above.

15. Claims 26-29 do not recite limitations above the claimed invention set forth in claims 1-4, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 1-4 above.

16. Claims 35-38 are rejected under 35 U.S.C. 102 (b) as being clearly anticipated by Parady, US Patent 5,933,627.

17. Referring to claim 35, Parady have taught a method comprising:

a. setting a tag of a register when an instruction having the register as a destination results in a cache miss, to identify the register as containing a scratch value (Figure 2, element 80);

b. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value until at least one instruction is detected that results in a cache miss (abstract, Thread 0 is bypassed when Thread 3 is executing until thread 3 experiences a cache miss.); and

c. re-executing bypassed instructions once a cache is loaded with cache miss data (abstract, Figure 3, column 3, line 35-column 4, line 64, The threads are switched in a round robin fashion. Thread 0 is reexecuted each time after threads 1, 2, and 3 finish executing. Thread 0 is reexecuted many times after the cache is loaded with the miss data.).

18. Referring to claim 36, Parady has taught the method of claim 35, as described above, and further comprising:

a. executing store instructions having a tag to indicate that the instruction involves a scratch value if tag values associated with operands of the store instruction indicate non-scratch values (Figure 2, column 3, lines 25-35, Instructions with valid tags are executed.).

19. Referring to claim 37, Parady has taught the method of claim 35, as described above, and further comprising:

a. propagating the tag to destination registers of the instructions to indicate that an operand within the destination registers is a scratch value (Figure 2, The tags are constantly maintained, and as such are propagated to the destination registers at all times.).

20. Referring to claim 38, Parady has taught the method of claim 35, as described above, and further comprising:

a. servicing detected cache miss instructions in parallel prior to re-executing the bypassed instructions (column 4, lines 41-52).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 12-15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al., US Patent 5,651,125, in view of Ebcioglu et al., US Patent 5,799.179.

23. Referring to claim 12, Witt et al. have taught a processor comprising:

a. at least two arithmetic units (Figure 6B, 840R, 845R);

b. a translation look aside buffer (Figure 6B, 915);

c. a branch prediction unit (Figure 6A, element 825); and

24. Witt et al. have not taught an execution engine having a plurality of instructions which when executed cause the processor to perform actions including:

a. identifying scratch values generated during speculative execution of a processor, and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value.

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value.

25. However, Ebcioglu et al. have taught taught an execution engine having a plurality of instructions which when executed cause the processor to perform actions including:

a. identifying scratch values generated during speculative execution of a processor (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16), and

b. setting at least one tag associated with at least one data area of the processor to indicate that the data area holds a scratch value (abstract, column 3, lines 31-631-61, column 4, lines 23-37, column 5, lines 1-7, column 5, lines 31-43, column 7, lines 5-16), for the desirable purpose of reducing the overhead from exceptions caused by speculative instructions (Ebcioglu et al., column 3, lines 58-61).

c. bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (column 4, lines 22-26, column 7, lines 13-16, column 9, lines 51-63, Tagged speculative instructions that are outside of the taken path are discarded, or bypassed, because they are no longer needed.)

26. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Witt et al. include the claimed execution engine and instructions, as taught by Ebcioglu, for the desirable purpose of reducing the overhead from exceptions caused by speculative instructions (Ebcioglu et al., column 3, lines 58-61).

27. Claims 13-15, 17, and 18 do not recite limitations above the claimed invention set forth in claims 2-4, 6, and 7 are respectively, and are therefore reject ed for the same reasons set forth in the rejection of claims 2-4, 6, and 7 above.

Allowable Subject Matter

28. Claims 5, 16, 23, 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

29. Claims 31-34 are allowed.

Response to Arguments

30. Applicant's arguments filed August 24, 2004 have been fully considered but they are not persuasive.

31. On pages 10-14, Applicants argue with respect to claims 1, 26, and 12 in essence:

> *"Ebcioglu or the references of record have not taught bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value. ... Applicant respectfully submits that the resetting of the exception bit by non-speculative instructions or speculative instructions, which do not require an exception, provides no teachings or suggestions with regards to bypassing execution of instructions having at least one operand that is a scratch value."*

Applicant may be correct that "the resetting of the exception bit by non-speculative instructions or speculative instructions, which do not require an exception, provides no teachings or suggestions with regards to bypassing execution of instructions having at

least one operand that is a scratch value". However, Ebcioglu et al. have taught bypassing execution of instructions having at least one operand with an associated tag that indicates that the operand is a scratch value (Tagged speculative instructions that are outside of the taken path are discarded or bypassed, column 4, lines 23-37). Therefore this argument is moot.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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